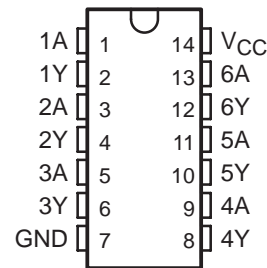


CD74ACT14 HEX SCHMITT-TRIGGER INVERTER

SCHS319A – NOVEMBER 2002 – REVISED NOVEMBER 2004

- Inputs Are TTL-Voltage Compatible
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Greater Noise Immunity Than Standard Inverters
- Operates With Much Slower Than Standard Input Rise and Fall Slew Rates
- ± 24 -mA Output Drive Current
 - Fanout to 15 F Devices
- SCR Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

E OR M PACKAGE
(TOP VIEW)



description/ordering information

The CD74ACT14 contains six independent inverters. This device performs the Boolean function $Y = \bar{A}$.

Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

ORDERING INFORMATION

| T _A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------|---------------|-----------------------|------------------|
| –55°C to 125°C | PDIP – E | Tube | CD74ACT14E | CD74ACT14E |
| | SOIC – M | Tube | CD74ACT14M | ACT14M |
| | | Tape and reel | CD74ACT14M96 | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each inverter)

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

logic diagram, each inverter (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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CD74ACT14

HEX SCHMITT-TRIGGER INVERTER

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage range, V_{CC} | -0.5 V to 6 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ± 50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 50 mA |
| Continuous current through V_{CC} or GND | ± 100 mA |
| Package thermal impedance, θ_{JA} (see Note 2): E package | 80°C/W |
| M package | 86°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | $T_A = 25^\circ\text{C}$ | | -55°C TO 125°C | | -40°C TO 85°C | | UNIT |
|--|--------------------------|----------|---|----------|--|----------|------|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| V_{CC} Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V_I Input voltage | 0 | V_{CC} | 0 | V_{CC} | 0 | V_{CC} | V |
| V_O Output voltage | 0 | V_{CC} | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} High-level output current | | -24 | | -24 | | -24 | mA |
| I_{OL} Low-level output current | | 24 | | 24 | | 24 | mA |
| $\Delta t/\Delta v$ Input transition rise or fall rate | | 20 | | 20 | | 20 | ns/V |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



CD74ACT14 HEX SCHMITT-TRIGGER INVERTER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | T _A = 25°C | | -55°C TO 125°C | | -40°C TO 85°C | | UNIT |
|--|---|---------------------------------------|-----------------|-----------------------|-----|----------------|-----|---------------|-----|------|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| V _{T+} Positive-going threshold | | | 5 V | 1.4 | 2 | 1.4 | 2 | 1.4 | 2 | V |
| V _{T-} Negative-going threshold | | | 5 V | 0.8 | 1.3 | 0.8 | 1.3 | 0.8 | 1.3 | V |
| ΔV _T Hysteresis (V _{T+} - V _{T-}) | | | 5 V | 0.4 | | 0.4 | | 0.4 | | V |
| V _{OH} | V _I = V _{T+} | I _{OH} = -50 μA | 4.5 V | 4.4 | | 4.4 | | 4.4 | | V |
| | | I _{OH} = -24 mA | 4.5 V | 3.94 | | 3.7 | | 3.8 | | |
| | | I _{OH} = -50 mA [†] | 5.5 V | | | 3.85 | | | | |
| | | I _{OH} = -75 mA [†] | 5.5 V | | | | | 3.85 | | |
| V _{OL} | V _I = V _{T-} | I _{OL} = 50 μA | 4.5 V | 0.1 | | 0.1 | | 0.1 | | V |
| | | I _{OL} = 24 mA | 4.5 V | 0.36 | | 0.5 | | 0.44 | | |
| | | I _{OL} = 50 mA [†] | 5.5 V | | | 1.65 | | | | |
| | | I _{OL} = 75 mA [†] | 5.5 V | | | | | 1.65 | | |
| I _I | V _I = V _{CC} or GND | | 5.5 V | ±0.1 | | ±1 | | ±1 | | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | | 5.5 V | 4 | | 80 | | 40 | | μA |
| ΔI _{CC} [‡] | V _I = V _{CC} - 2.1 V | | 4.5 V to 5.5 V | 2.4 | | 3 | | 2.8 | | mA |
| C _i | | | | 10 | | 10 | | 10 | | pF |

[†] Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

[‡] Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

ACT INPUT LOAD TABLE

| INPUT | UNIT LOAD |
|-------|-----------|
| A | 0.21 |

Unit load is ΔI_{CC} limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -55°C TO 125°C | | -40°C TO 85°C | | UNIT |
|------------------|--------------|-------------|----------------|------|---------------|------|------|
| | | | MIN | MAX | MIN | MAX | |
| t _{PLH} | A | Y | 3.6 | 14.5 | 3.7 | 13.2 | ns |
| t _{PHL} | | | 2.4 | 9.5 | 2.4 | 8.6 | |

operating characteristics, V_{CC} = 5 V, T_A = 25°C

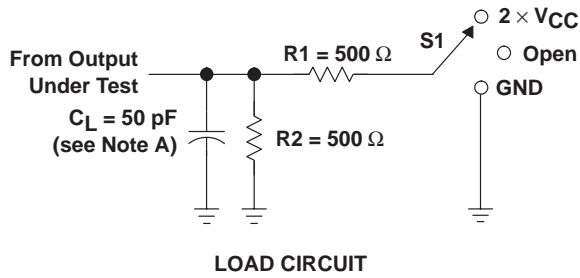
| PARAMETER | TYP | UNIT |
|---|-----|------|
| C _{pd} Power dissipation capacitance | 45 | pF |



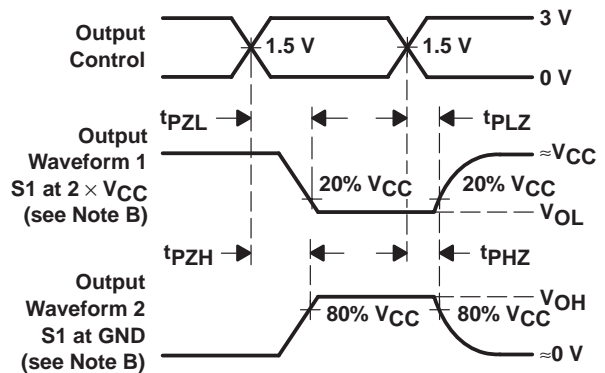
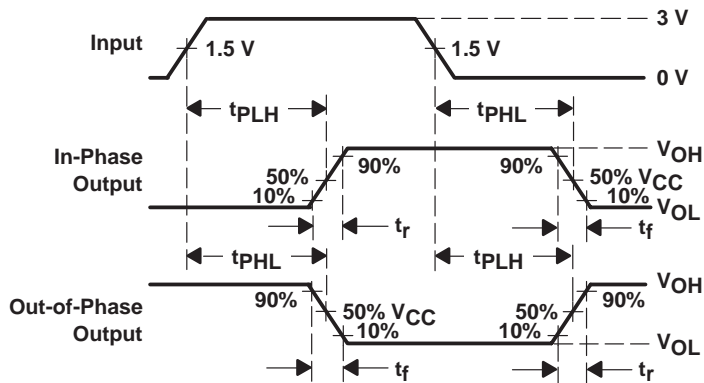
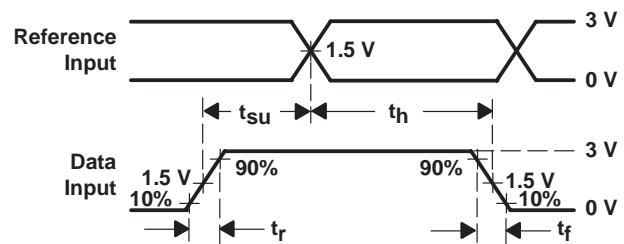
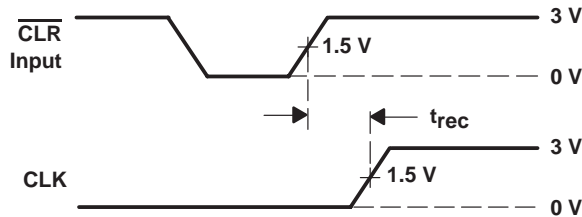
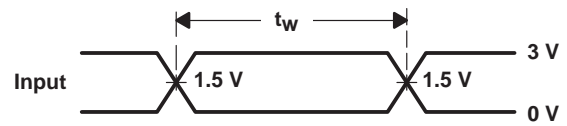
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PARAMETER MEASUREMENT INFORMATION



| TEST | S1 |
|-------------------|-------------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |



- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$. Phase relationships between waveforms are arbitrary.
 - For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - The outputs are measured one at a time, with one input transition per measurement.
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD74ACT14E | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74ACT14E | Samples |
| CD74ACT14M | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT14M | Samples |
| CD74ACT14M96 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT14M | Samples |
| CD74ACT14MG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT14M | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74ACT14M96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

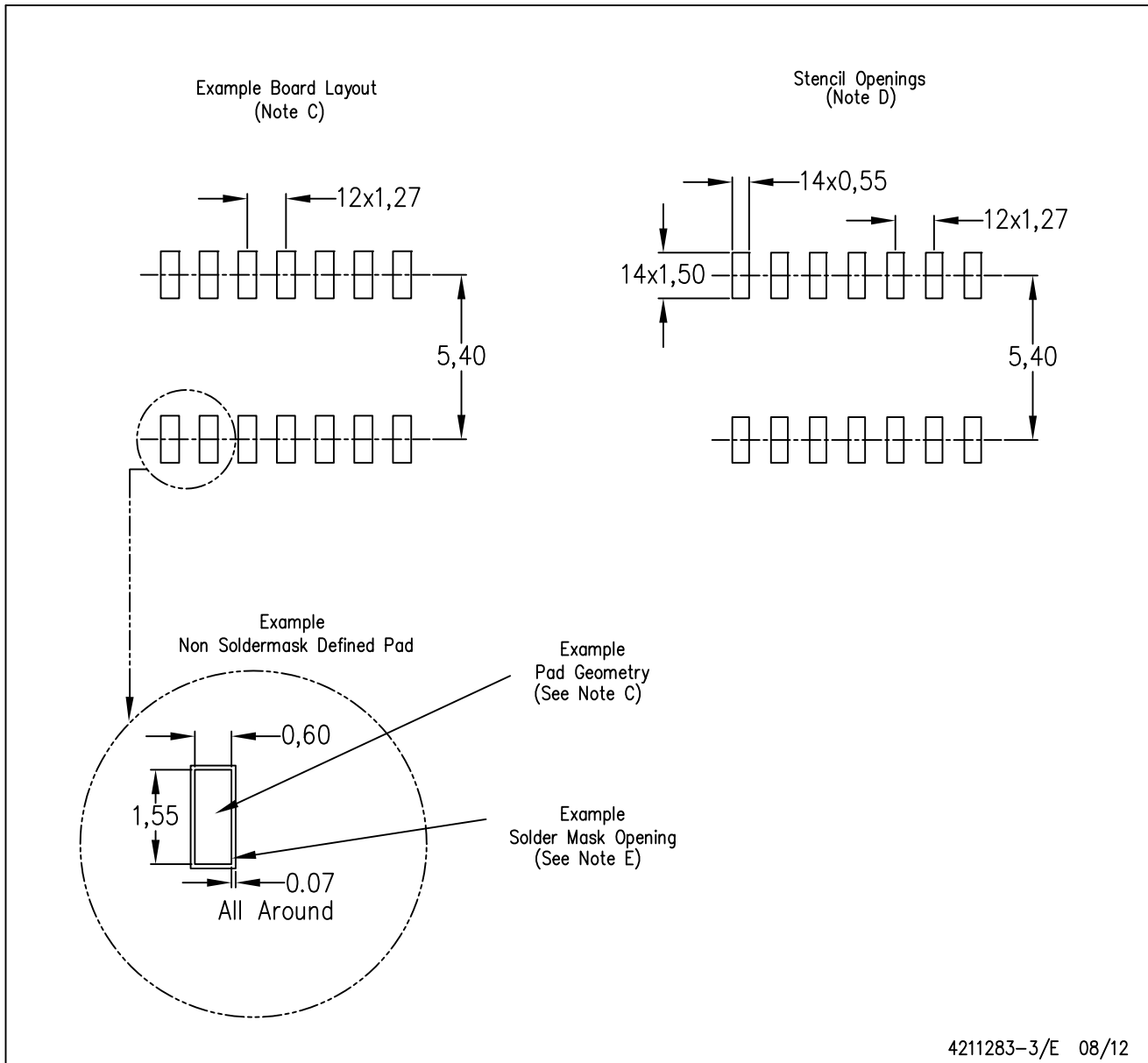


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74ACT14M96 | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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